Remarks

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claims 1-5 and 15-18 are presented for examination. Previously presented claims 6-14 have been canceled. Independent claims 1 and 15 include the feature of a semiconductor element area, with a plurality of semiconductor elements, and a dummy semiconductor element area, with a plurality of dummy semiconductor elements, that surrounds the semiconductor area. This is supported, for example, in the discussion of Fig. 5 at col. 5, ,lines 16-30. New claim 16 tracks previous claim 7. New claim 17 is supported, for example, at col. 8, line 10. New claim 18 is supported, for example, at col. 4, line 46 and col. 6, lines 60-61.

Claims 1-14 were rejected as based on a defective reissue Declaration. A substitute reissue Declaration is provided. Applicants respectfully contend that the Declaration adequately identifies at least one error relied upon for the reissue application. The executed version of the substitute Declaration will be submitted shortly.

Claims 6-14 were rejected as being improper recapture of subject matter surrendered during prosecution of the parent application. This issue is rendered moot by the cancellation of claims 6-14; Applicants are not conceding the correctness of the rejection. Applicants respectfully traverse the rejection were it to be applied to claims 15-18. As noted above, independent claim 15 includes the feature of the semiconductor element area and the dummy semiconductor element area from col. 5 and Fig. 5. There was no "surrender" in the parent prosecution relative to this feature.

Claims 6, 8, 11 and 14 were rejected as anticipated by Tahaishi. This rejection is rendered moot by the cancellation of the rejected claims. Applicants are not conceding the correctness of the rejection. Takaishi fails to disclose or even suggest the semiconductor element area and dummy semiconductor element area required by claim 15. This arrangement is advantageous in that, due to the presence of the dummy semiconductor element area around the semiconductor element area, the top electrodes of the dummy semiconductor elements limit the exposure of the dielectric surface of the semiconductor element to impact from etching ions. This helps to suppress the degradation of the dielectric film. See Figs. 17 and 18 of the present application and the

accompanying discussion at col. 8. Takaishi thus suggests neither the structure of claim 15 nor the advantages achieved with the structure.

Claims 1, 2, 5-10 and 13 were rejected as obvious over Tsuchiya in view of Uehara. Applicants note that Tsuchiya was omitted from the PTO 892 form, and request that it be listed. Applicants respectfully traverse the rejection. Like Takaishi, neither Tsuchiya nor Uehara discloses or suggests the semiconductor element area and dummy semiconductor element area of independent claims 1 and 15. Therefore, the rejection should be withdrawn.

Favorable reconsideration in the form of a Notice of Allowance is requested.

Respectfully submitted,

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